REMARKS

Claims 1-20 are currently pending, of which claims 1, and 14-18 are independent. Claims 5-6, 14-15, and 18 are currently amended. No new matter is added. Reconsideration of the action mailed February 7, 2006, is respectfully requested in light of the foregoing amendments and the following remarks.

The Examiner has rejected claims 5, 14, 15, 19, and 20 under 35 U.S.C. § 112, second paragraph as being indefinite. The Examiner has rejected claims 1-5, 12, and 14-20 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,607,313 to Farries et al. (hereinafter "Farries") in view of U.S. Patent No. 6,256,124 to Hait (hereinafter "Hait"). Applicant respectfully traverses the rejections.

Section 112 Rejections

The Examiner rejected claims 5, 14, 15, 19, and 20 under 35 U.S.C. § 112, second paragraph as being indefinite. Specifically, the Examiner rejected claims 5, 14, and 15 as including features lacking antecedent basis. Claims 19 and 20 were rejected based on their dependency from claim 14. Applicant has amended claims 5, 14, and 15 to correct antecedent basis and therefore respectfully submits that the § 112 rejection of claims 5, 14, 15, 19, and 20 has been overcome.

Section 103(a) Rejections

Claim 1 stands rejected over Farries and Hait. Claim 1 is directed to an integrated optical time division multiplexing module that includes an integrated time-delay chip. The integrated time-delay chip introduces an optical delay between at least a first and second optical Return-to-Zero signal streams. The integrated time-delay chip includes a plurality of waveguides formed on a substrate of the integrated time-delay chip for introducing the optical delay. The integrated time-delay chip is also operable to combine optical Return-to-Zero signal streams including interleaving the plurality of waveguides on the integrated time-delay chip.

The Examiner states that Farries fails to disclose an integrated time-delay chip including a plurality of waveguides formed on a substrate of the integrated time-delay chip, but that Hait does at FIG. 1 and col. 8, lines 47-58. Applicant respectfully disagrees.

FIG. 1 of Hait discloses a block diagram of a time division multiplexer that includes a number of separate blocks titled "Delay Means" coupled to separate optical modulators. Hait does not disclose or suggest the structure of the proposed delay means used to apply a time delay to optical signals. More specifically, Hait does not disclose or suggest a plurality of waveguides, which are all formed on a substrate of an integrated time-delay chip.

Col. 8, lines 47-58 of Hait includes a list of possible delay means that can be used, including, "free-space distances, materials having an index of refraction greater than one, waveguides, optical fibers, one-shot multivibrators" (*see* col. 8, lines 48-50). Hait only discloses a list of distinct components that can be used to provide a time-delay for an optical signal. However, Hait does not disclose or suggest an integrated time-delay chip that includes a plurality of waveguides formed on a substrate of the integrated time-delay chip. A list of separate delay components, which include waveguides, does not disclose or suggest the particular integrated time-delay chip structure of claim 1 where a plurality of waveguides are formed on a substrate of a single integrated chip. Furthermore, the disclosure in Hait of the existence of waveguides as a possible means for providing a time delay fails to disclose or suggest a structure in which a plurality of waveguides are interleaved within an integrated time-delay chip for combining optical signals, as required by claim 1.

The examiner also states that Farries discloses interleaving the plurality of waveguides on the integrated time-delay chip at col. 5, lines 63-66. Applicant respectfully disagrees. Lines 63-66 of col. 5 of Farries provide, in pertinent part, as follows:

> The birefringent crystal for use as a polarization combiner and delay line for time-division polarization interleaving of pulses.

The cited section of Farries discloses the combining of optical signals using a birefringent crystal. Light signals enter the birefringent crystal at different locations. Orthogonal polarizations of the light signals cause a first light signal to deflect and converge with a second optical signal. However, this convergence occurs within a birefringent crystal, which is a separate component from Farries' time-delay structure. In contrast, the integrated time-delay chip of claim 1 performs both delay and combining functions. Additionally, the birefringent crystal of Farries merges optical signals passing through a crystal and does not disclose or suggest Applicant's claimed interleaving waveguides that are formed into the substrate of an integrated time-delay chip.

Furthermore, light passing through a crystal has a path based on the point of entry and the properties of the light and crystal. Thus, there can be multiple paths through a given crystal. However, a waveguide formed on substrate is a particular guide constructed for light signals to pass through a material. Therefore, crystal paths are not the same as the claimed waveguides. Applicant respectfully submits that claim 1, as well as claims 2-13, which depend from claim 1, are in condition for allowance.

Claim 14 stands rejected over Farries and Hait. Claim 14 is directed to an integrated optical time division multiplexing module that includes an integrated time-delay chip including first and second waveguides formed on a substrate where one of the waveguides has a greater length than the other waveguide. The integrated time-delay chip is operable to combine the first and second optical signals including interleaving the first and second waveguides. For at least the reasons set forth above with respect to claim 1, claim 14, as well as claim 19, which depends from claim 14, are in condition for allowance.

Claim 15 stands rejected over Farries and Hait. Claim 15 is directed to an integrated optical time division multiplexing module that includes an integrated time-delay chip that includes first and second waveguides formed on a substrate where one of the waveguides has a greater length than the other waveguide. The difference in length provides a particular time-delay to signals passing through the longer waveguide with respect to the other waveguide. As discussed above, Farries does not disclose or suggest an integrated time-delay chip including

waveguides written into a substrate. Additionally, Hait does not disclose or suggest a plurality of waveguides written into the substrate of an integrated time-delay chip where one waveguide is longer than the other. The disclosure in Hait of the existence of waveguides as a possible delay means does not disclose waveguides written into a substrate of an integrated time delay chip. Applicant respectfully submits that claim 15 as well as claim 20, which depends from claim 15, are in condition for allowance.

Claim 16 stands rejected over Farries and Hait. Claim 16 is directed to an integrated optical time division multiplexing module that includes an integrated time-delay chip that includes first and second waveguides formed on a substrate of the integrated time-delay chip. For the reasons set forth above with respect to claim 15, claim 16 is in condition for allowance.

Claim 17 stands rejected over Farries and Hait. Claim 17 is directed to an integrated optical time division multiplexing module that includes first and second waveguides formed on a substrate of the integrated time-delay chip. For the reasons set forth above with respect to claim 15, claim 17 is in condition for allowance.

Claim 18 stands rejected over Farries and Hait. Claim 18 is directed to an integrated optical time division multiplexing module that includes integrated time-delay chip including a plurality of waveguides formed on a substrate of the integrated time-delay chip for introducing an optical delay and for combining optical Return-to-Zero signal streams where the optical Return-to-Zero signal streams are combined by interleaving the plurality of waveguides on the integrated time-delay chip. For the reasons set forth above with respect to claim 1, claim 18 is in condition for allowance.

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Applicant respectfully requests that all pending claims be allowed. Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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